

UTD Cochlear Implant Research Interface

Experimental Validation for Bilateral Synchronization

Claim: UTD CI Platform is bilaterally synchronized

i.e., it enables perfectly synchronized stimulation for both left and right implants (in other words, there is no delay in stimulation pulses between the left and right implant.)

Experimental Protocol:

- Two similar implant emulators (model # CI24RE) were used.
- A stream of constant-amplitude pulses was sent from the PDA/smartphone.
- Output at the receiver coils and electrodes was verified using oscilloscope.

Experiment 1: Measure RF output of the receiver coil

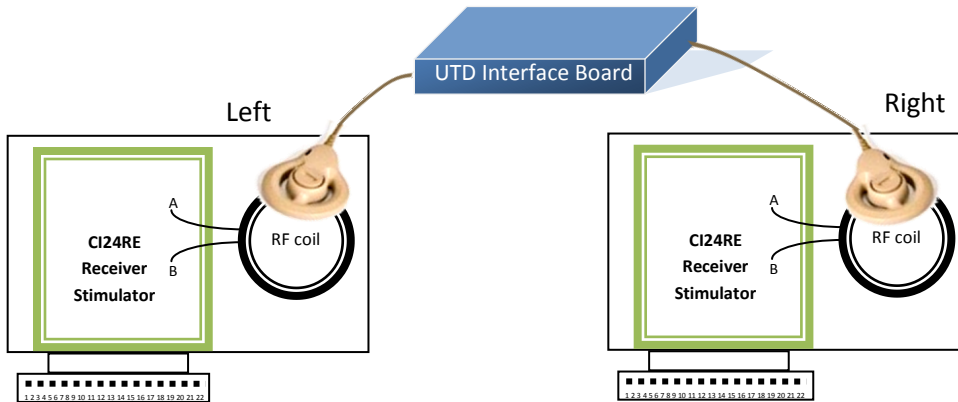
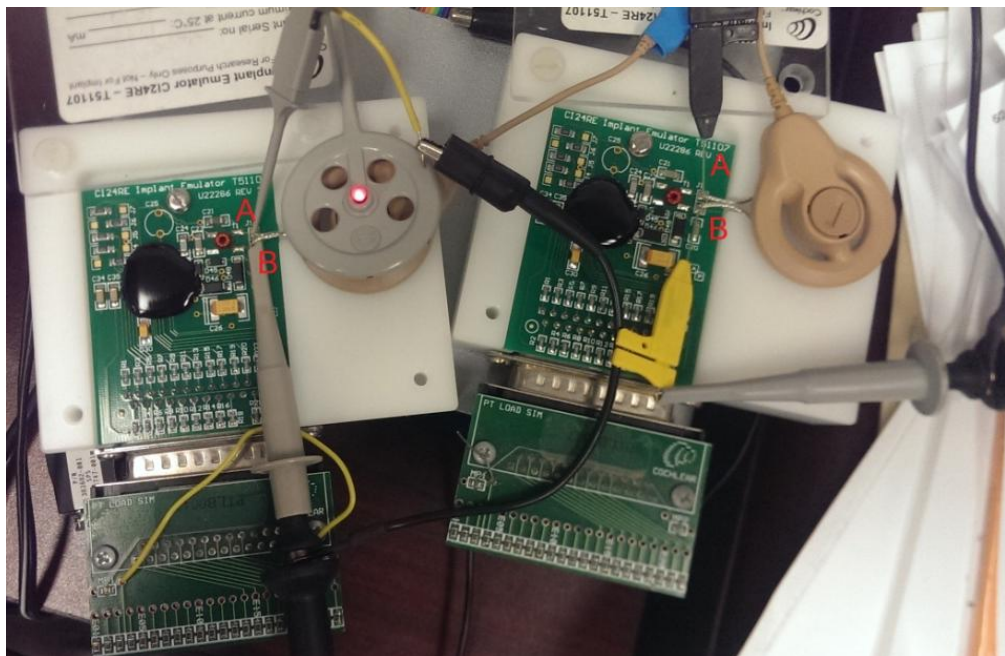


Figure 1: Using CI24RE Emulators, RF frames were directly probed at points (A, B)



Results:

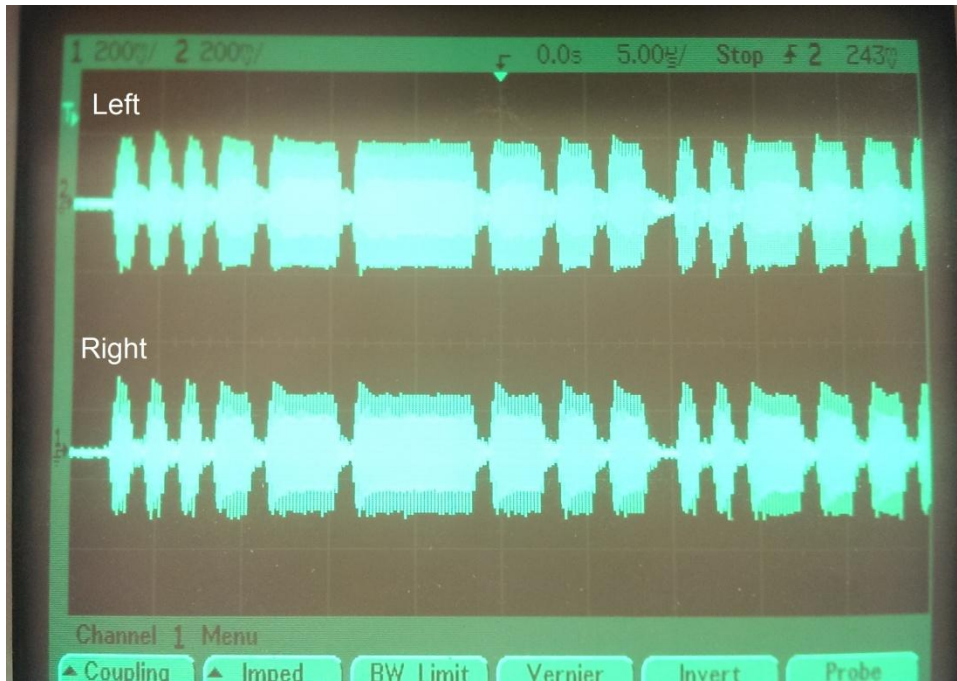


Figure 2: RF Frames for left and right (probe point A, B)

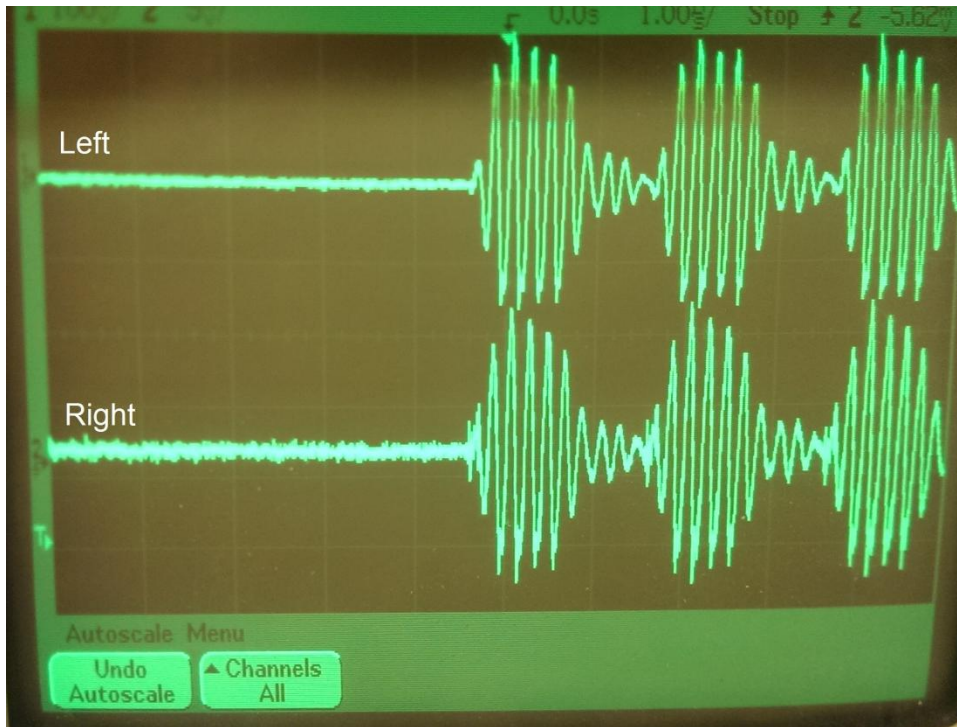
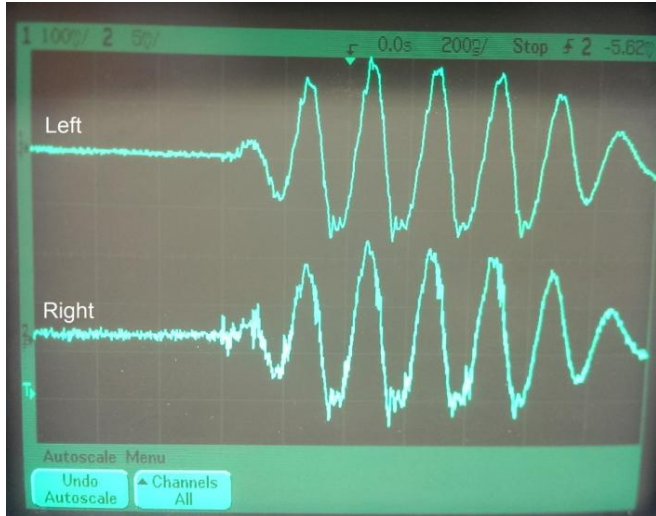
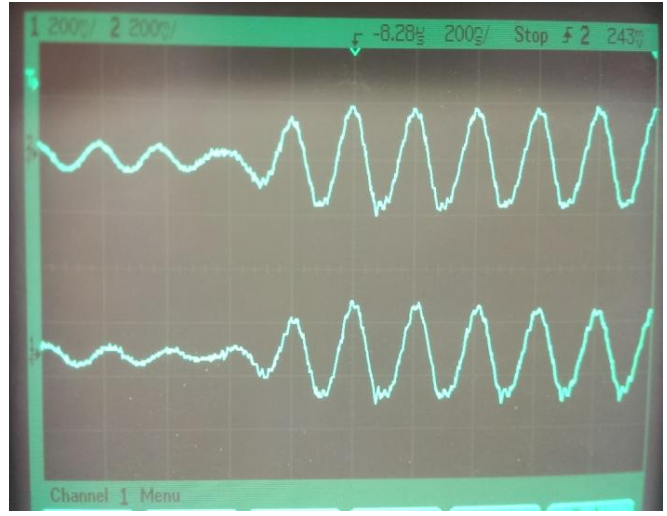


Figure 3: Magnified version of RF frames for left and right

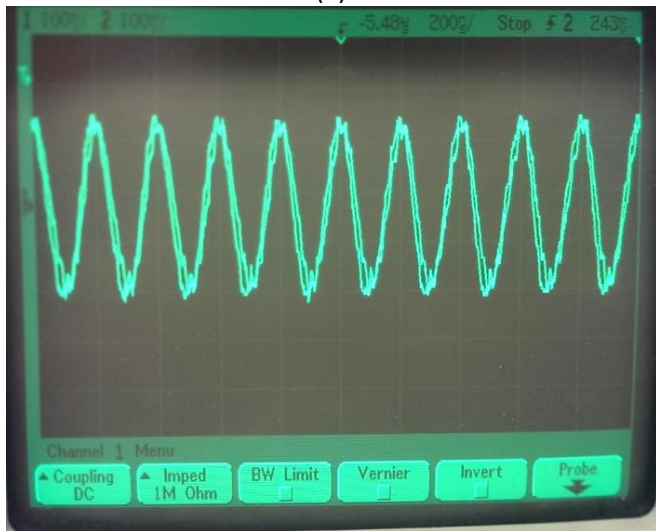
Experimental validation for bilateral synchronization of UTD CI processor



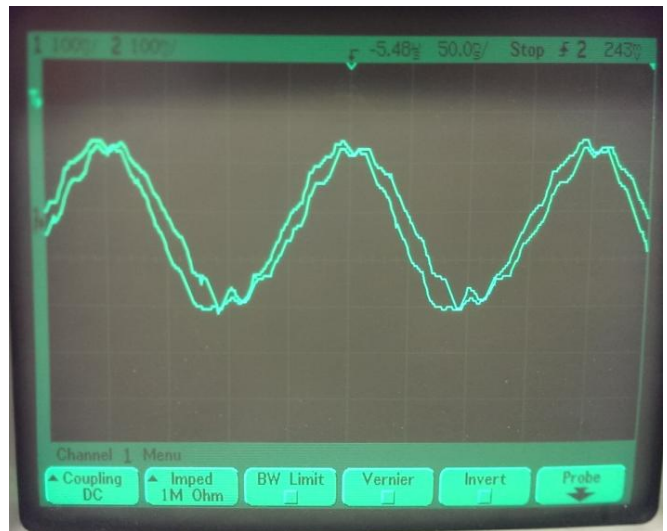
(a)



(b)



(c)



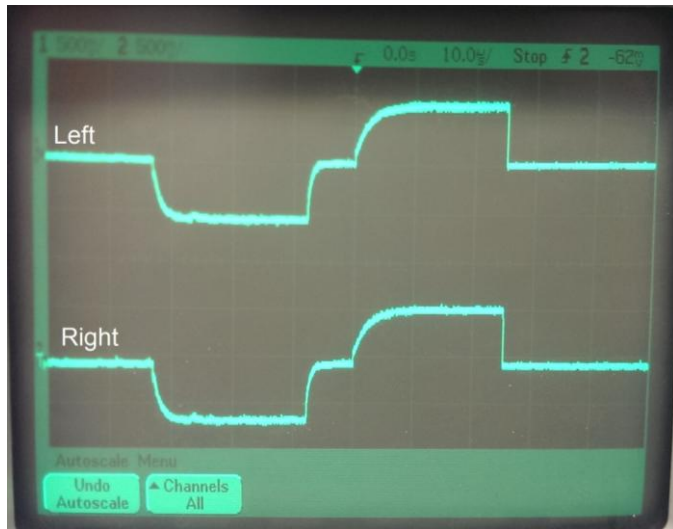
(d)

Figure 4: Magnified version of RF waveforms for left and right.
(c) and (d) both left and right RF waveforms are superimposed on each other.

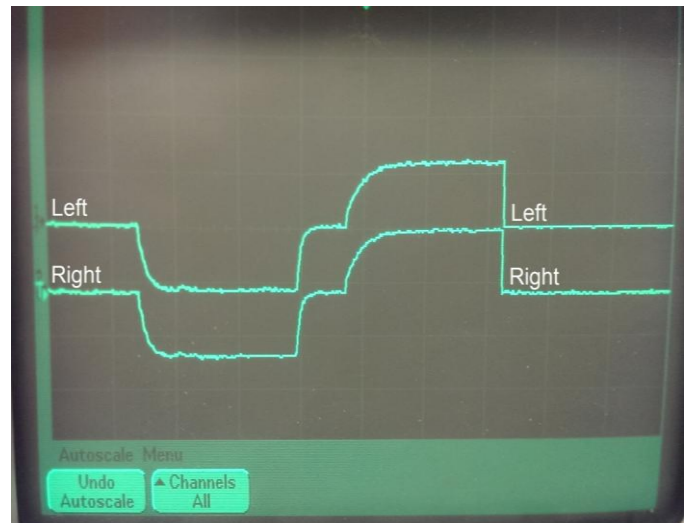
Experiment 2: Probe output stimuli

In this experiment, Electrode 1 of both left and right sides was probed for biphasic pulses using two implant emulators and output was viewed on the oscilloscope.

Results:



(a)



(b)

Figure 5: Individual biphasic pulses from left and right sides for electrode # 1 indicating synchronization in time

Conclusion:

The experimental data indicates that RF frames and output pulses are synchronized in time (i.e., there is no latency between the onset/offset of pulses at either side).

The experimental data bolsters the system design of the UTD CI interface board. The FPGA sends out RF frames to both left and right sides at the same time. The parallel architecture of the FPGA hardware allows time synchronized processing in a convenient way.