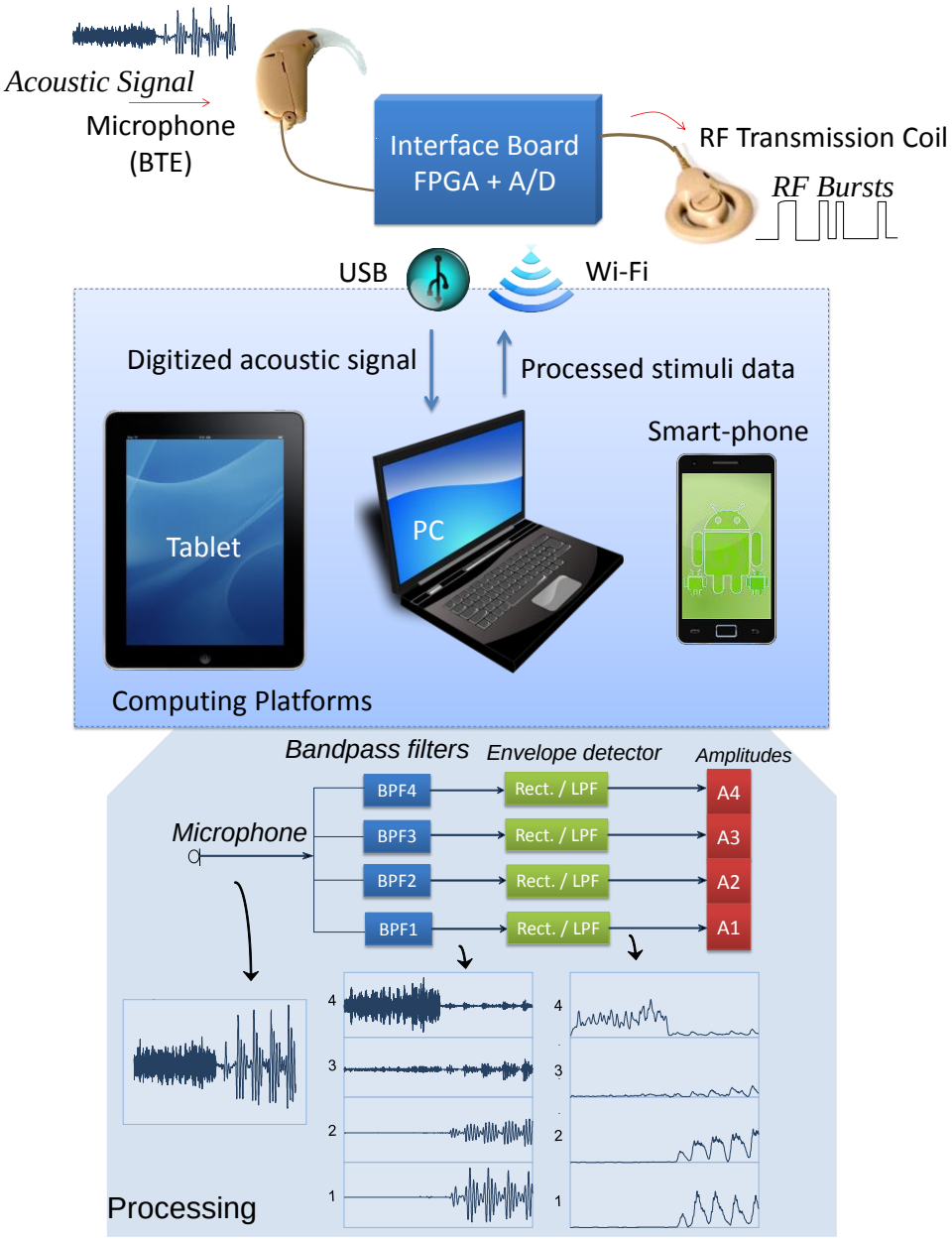
UT-Dallas Cochlear Implant Research Interface

System Level Design

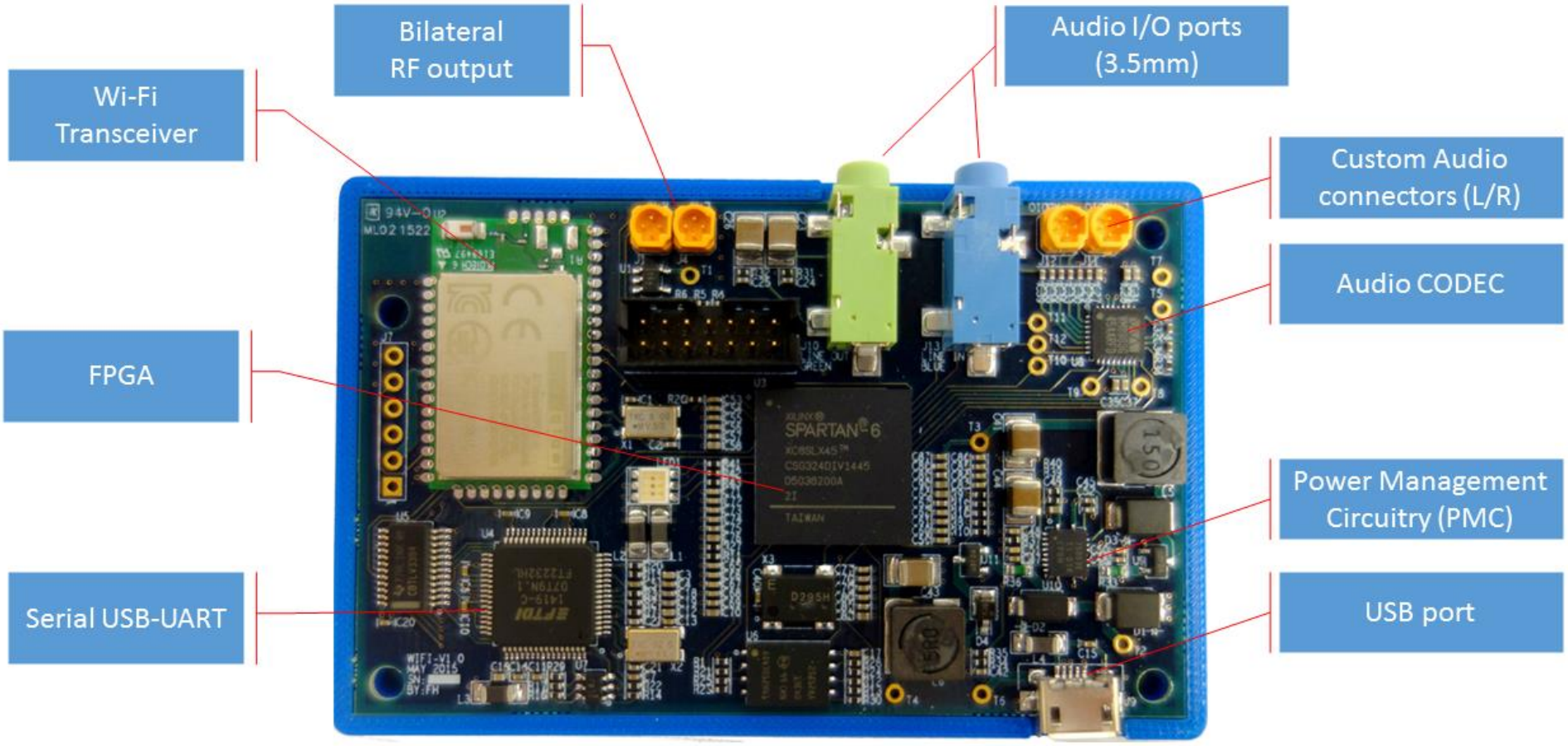
Cochlear Implant Laboratory

High Level Description

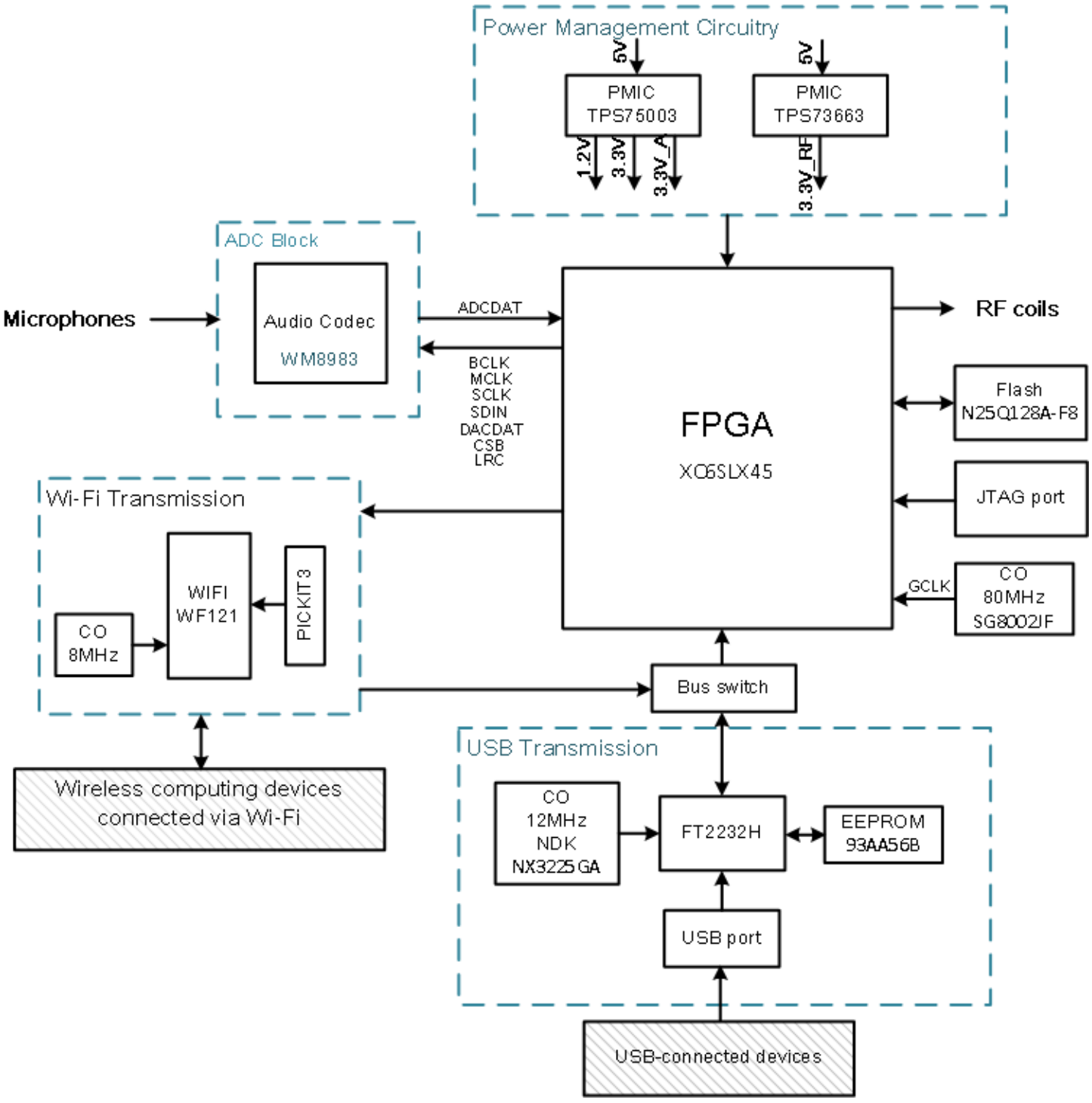


- The acoustic signal is first acquired from Behind-the-Ear (BTE) unit and is sampled digitally by an on-board stereo codec. The sampled signal is transmitted to the computing platform either wirelessly (over Wi-Fi) or via USB-serial port.
- The computing platform, which could either be a personal computer (PC) or a portable device, such as a smartphone/tablet, receives packets of stereo acoustic data, and processes them through a sound coding strategy on a frame-by-frame basis (every 8 ms).
- As a proof-of-concept, Advanced Combination Encoder (ACE) strategy has been implemented.
- The processing generates a set of stimulation sequence which consists of electrode, mode, amplitude (EMA), and timing of each biphasic pulse. This stimulation data is sent back to the interface board where it is encoded (using the transmission protocols of the CI device) in the FPGA, and is finally streamed to the implant for stimulation.
- The process is repeated in realtime.

Hardware

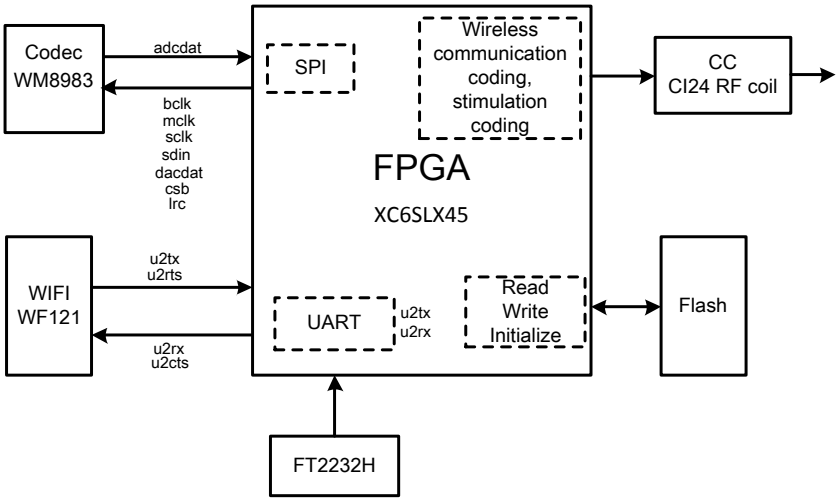

Bilateral
RF output
Audio I/O ports
(3.5mm)
Wi-Fi
Transceiver
Custom Audio
connectors (L/R)
Audio CODEC
FPGA
Power Management
Circuitry (PMC)
Serial USB-UART
USB port

Functional Diagram



Hardware Components

FPGA: The central processor is a Field Programmable Gate Array (FPGA) from Xilinx (XC6SLX45). FPGA controls the data flow in the system. It is responsible for synchronized capture of audio frames from the codec, two-way data transfer, encoding of RF data, and synchronized delivery of stimulation pulses to the RF coils. The Wi-Fi and USB transmission blocks communicate with the core FPGA using UART standard protocol, while the audio codec uses the SPI protocol for data exchange. In addition to the RF encoding, FPGA firmware also realizes safety checks for safe stimulation delivery. The FPGA is programmed in Verilog, locked, and not accessible to the researchers.



Audio Codec: The audio codec from Wolfson Microelectronics (WM8983) is a highly integrated input/output device designed for mobile computing and communications. The device integrates preamps for stereo differential mics, and includes drivers for speaker, headphone and differential or stereo line output. External component requirements are reduced as no separate microphone or headphone amplifiers are required. Advanced on-chip digital signal processing includes a 5-band equalizer, a mixed signal Automatic Level Control for the microphone or line input through the ADC as well as a purely digital limiter function for record or playback. A programmable high pass filter in the ADC path is provided for wind noise reduction and an IIR with programmable coefficients can be used as a notch filter to suppress fixed-frequency noise. Key features of the audio codec are as follows:

ADC	**4 channels**
SNR	87 dB
AGC	Yes
Interfaces	PCM, I^2S
Power Supply	1.8 – 3.6 V
Package	7 × 7 mm 48-pin QFN

Wi-Fi Transceiver: The Wi-Fi transceiver from Bluegiga (WF121) is a stand-alone Wi-Fi module that provides fully integrated 2.4GHz 802.11 b/g/n radio, TCP/IP stack and a 32-bit micro controller (MCU) platform for simple, low-cost and low-power wireless IP connectivity. It also provides flexible peripheral interfaces such as SPI, I2C, ADC, GPIO, Bluetooth co-existence, and timers to connect various peripheral interfaces directly to the WF121 Wi-Fi module.

Key Features:

- 2.4GHz band IEEE 802.11 b/g/n radio
- Radio performance: TX power: +17 dBm, RX sensitivity: -97 dBm
- Host interfaces: 20Mbps UART, USB on-the-go
- Peripheral interfaces: GPIO, AIO and timers, I2C, SPI and UART, Ethernet

- Embedded TCP/IP and 802.11 MAC stacks: IP, TCP, UDP, DHCP and DNS protocols, BGAPI host protocol for modem like usage, BGScriptTM scripting language or native C-development for self-contained applications
- 32-bit embedded microcontroller: 80MHz, 128kB RAM and 512kB Flash, MIPS architecture
- Fully CE, FCC and IC qualified

USB Interface: The FT2232H is a USB 2.0 Hi-Speed (480Mb/s) to UART/FIFO IC that is used for direct connect mode to interface PC and portable USB-based devices with the board via a micro-USB connector.

Power Management: The circuit board runs from a 5-V battery which connects to the micro-USB port of the board. The power management circuitry comprises of two main components: TPS75003 and TPS73663. The TPS75003 is an integrated triple supply power management IC (PMIC) for the Xilinx Spartan FPGA and regulates voltage and current levels of the digital part of the circuit board. The TPS73663 is a low-dropout (LDO) regulator and is used to provide stable power to the RF analog circuitry. The use of two separate LDOs ensures lower cross-interference between the digital and analog circuitries.