31st Annual International Conference of the IEEE EMBS
Minneapolis, Minnesota, USA, September 2-6, 2009

Laboratory Prototype of Cochlear Implant: Design and Techniques

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***Abstract*—This paper presents design overview of a low cost prototype of Cochlear Implant developed from commercial off-the-shelf components. Design scope includes speech processing module implemented on a commercial digital signal processor, transcutaneous data and power transceiver developed from a single pair of inductive coils and finally a stimulator circuitry for cochlear stimulation. Different speech processing strategies such as CIS, SMSP and F0/F1 have been implemented and tested using a novel, indigenously developed speech processing research module which evaluates the performance of speech processing strategies in software, hardware and practical scenarios. Design overview, simulations and practical results of an optimized inductive link using Class E Power Amplifier are presented. Link was designed at a carrier frequency of 2.5MHz for 100mW output power. Receiver logic design and stimulator circuitry was implemented using a PIC microcontroller and off-the-shelf electronic components. Results indicate 40% link efficiency with 128kbps data transfer rate. This low cost prototype can be used for undertaking cochlear implant research in laboratories.**

I. Introduction

Cochlear Implant (CI) is one of the most popular and successful prosthetic devices in terms of performance and demand. It is a device which restores hearing to the patients with conductive as well as sensory-neural hearing loss. CI mimics functionality of a healthy cochlea by bypassing the natural hearing mechanism and directly stimulating the inner ear sensory cells of the auditory nerve by delivering electrical signals to an electrode array implanted inside the cochlea. Fig. 1 shows the block diagram of the complete CI system.

Sound is acquired through a microphone which is then processed in a speech processor. Speech processor is essentially a digital signal processor programmed with different speech processing strategies. All speech processing strategies usually split the acquired sound signal into different frequency bands called channels, before compressing and converting them into biphasic pulses. Performance of these strategies varies from language, tone and person to person. Data from these channels is coded, multiplexed and modulated before it is finally transmitted through a transcutaneous link in the form of electromagnetic waves to the inner ear. Logic circuitry at the receiver end receives the data, demodulates it, decodes it and finally de-multiplexes it before sending the pulses to the stimulator circuitry which finally converts these logic signals into biphasic current pulses. These current pulses are provided to an electrode array implanted inside cochlea.

Details of speech processing module, speech processing algorithms and their implementation in hardware are discussed in Section II. Section III provides design details of the inductive link and power amplifier. Receiver-stimulator logic and electronic circuitry is presented in Section IV. Simulation and practical results are then given in Section V followed by conclusion.

Manuscript received April 23, 2009.

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II. Speech Processing

A speech processing strategy is one of the key features which affect the overall performance of CI [1]. Various strategies have been developed and reported in literature over time for cochlear prosthesis which include Continuous Interleaved Sampling (CIS), Spectral Peak (SPEAK), Advanced Combination Encoder (ACE) , Spectral Maxima Sound Processor (SMSP) [1-4].

We implemented CIS, F0/F1 and SMSP for eight channel implant on TI C6713 DSP. Algorithms were initially developed and tested in MATLAB and SIMULINK and then finally coded in C using Code Composer Studio before they were finally realized on the processor. A considerable effort was done to keep the computation cost as low as possible by using multirate, multistage filters and by performing all computations in frequency domain which resulted in cost reduction by more than 70% as compared to the use of conventional FIR filters in time domain. Details of the algorithm implementation can be found in [5]. Data from each band was then coded using the coding scheme given in Fig. 2. This simple coding scheme not only enabled easier synchronization and decoding but also uniform radio frequency energy transmission. Finally all the channels were framed, time multiplexed and the output from the DSP was transferred to the transcutaneous link.

In addition to this, a low-cost speech processing research module for the assessment and real-time evaluation of speech processing strategies and algorithms was developed using DSK TMS320C6713. This research module consists of three sub-modules: i) Software Evaluation Module, ii) Hardware Evaluation Module and iii) Real-time Patient Evaluation Module. This research module enables easy implementation, modification and assessment of any speech processing strategy or algorithm in software as well as its

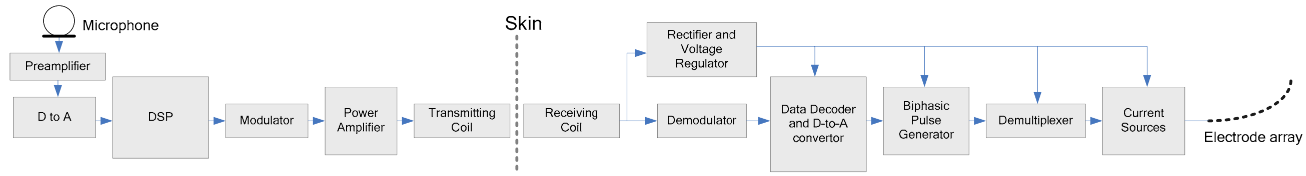


Fig. 1. Block diagram of complete Cochlear Implant system

realization in hardware. Real-time operational performance of the developed algorithms in hardware can be easily studied and adjusted using this research platform. Details of this module have been given in our previous paper in [6].

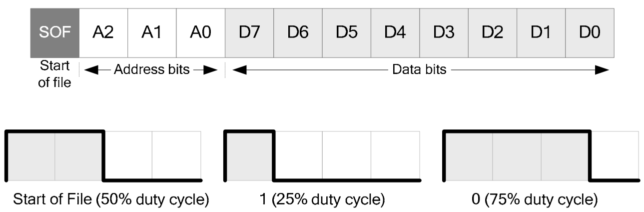


Fig. 2. Framing and coding scheme

III. TRANSCUTANEOUS LINK

Inductively coupled coils remain most popular choice for wireless data and power transmission. Design requirements of an inductive link for medical implant demands careful consideration of (i) bandwidth for supporting high data rates; (ii) efficiency for minimum power drop across the link; (iii) coupling insensitivity to coil misalignments; iv) form factor and v) biocompatibility. Data and power transmission have conflicting requirements in terms of efficiency. Wider bandwidth and high data rates are better supported at higher frequency. On the contrary, efficient power transfer is achieved using low operating frequency. Therefore, optimization of efficiency for power transfer is highly desirable due to low coupling in practical implants [7].

A. Mathematical Link Modeling

First step in the design and analysis of an inductive link is to compute link response at operating frequency. Primary circuit tuned in series resonance and secondary tuned in parallel resonance as shown in Fig. 3 is an ideal combination because phase of the inductor and capacitor voltage cancel at resonance and therefore a series-resonant primary network requires lower voltage swings at its input [8]. Equations governing the link efficiency and voltage gain are given by (1) and (2) respectively.

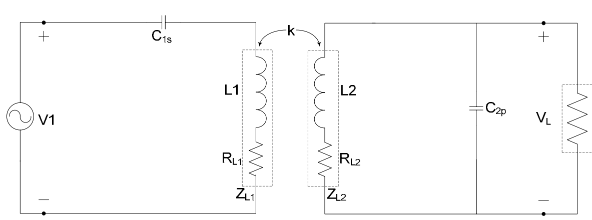


Fig. 3. Inductive link model

$$\eta_{link} = \frac{\omega^2 M^2 R_{load}}{\left(\boldsymbol{A}.R_{load}^2 C_{2p}^2\right)\omega^4 + \left(\boldsymbol{A} + \boldsymbol{B}.R_{L1}C_{2p}R_{load}^2\right)\omega^2 + \left(\boldsymbol{C}^2.R_{L1}\right)} \quad (1)$$

$$\frac{V_L}{V_1} = \frac{\omega^2 M C_{1s} R_{load}}{\left\{ \begin{matrix} -\left(\boldsymbol{D}.R_{load}C_{2p}C_{1s}\right)\omega^4 + jC_{1s}(\boldsymbol{E})\omega^3 + \\ (\boldsymbol{G})\omega^2 - j\left(\boldsymbol{F} + R_{load}C_{2p}R_{L2}\right)\omega^1 - \boldsymbol{C} \end{matrix} \right\}} \quad (2)$$

where,

$\boldsymbol{A} = (R_{L1}L_2^2 + R_{L2}M^2)$, $\boldsymbol{B} = (R_{L2}^2 C_{2p} - 2L_2)$,
$\boldsymbol{C} = (R_{L2} + R_{load})$, $\boldsymbol{D} = (M^2 - L_1 L_2)$,
$\boldsymbol{E} = \left(\boldsymbol{H}.C_{2p}R_{load} - \boldsymbol{D}\right)$, $\boldsymbol{F} = (\boldsymbol{C}.R_{L1}C_{1s} + L_2)$,
$\boldsymbol{G} = [C_{1s}(\boldsymbol{I}.R_{load} + \boldsymbol{H}) + R_{load}C_{2p}L_2]$,
$\boldsymbol{H} = (L_1 R_{L2} + L_2 R_{L1})$, $\boldsymbol{I} = (L_1 + R_{L1}R_{L2}C_{2p})$

B. Coil Design

Second step is coil design, which plays a critical role in optimum data and power transmission. Design factors which contribute to link efficiency and voltage gain include coupling coefficient, quality factor, coil geometry, coil dimensions, type of wire used in windings, inductance and number of turns. Details about the optimization of these parameters for maximum link efficiency can be found in [17]. In a nutshell, coupling coefficient and quality factor of coils should be maximized for maximum link efficiency.

1) Coil Design Process: Coil coordinates were first calculated in MATLAB and passed to Fast Henry, a Finite Element Analysis (FEA) software, to compute frequency-dependent self and mutual inductances, as well as parasitic resistances of generic three-dimensional conductive structures in the form of Z matrix. Extracted *z* parameters were again passed to MATLAB to compute value of coupling coefficient. Finally, SPICE was used to simulate the inductive link on extracted value of *k*. Depending on the output of SPICE, coil parameters were changed until optimal *k* was extracted.

TABLE I
COIL PARAMETERS AT PRIMARY AND SECONDARY SIDE

Primary	Secondary
L=80µH	L=8µH
$R_{effective}$=2.5Ω	$R_{effective}$=1.4Ω
$Q_{unloaded}$=350	$Q_{unloaded}$=89
N=45	N=24
$R_{external}$=13.5mm	$R_{external}$=6.3mm
$R_{internal}$=7.5mm	$R_{internal}$=3.3mm

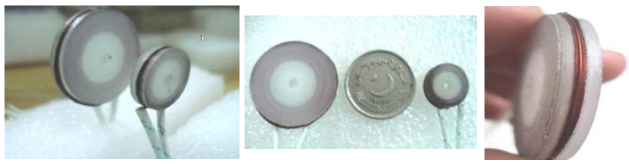


Fig. 4. Inductive Coils

Circular planar coils based on the given principles were designed for the transcutaneous link as shown in Fig. 4. Relevant design parameters of the coil are given in Table I.

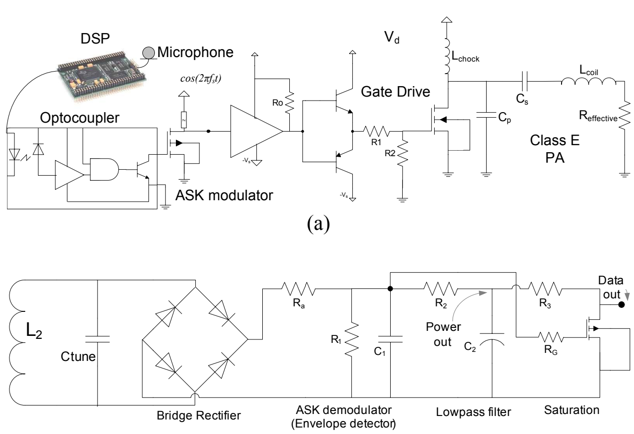
C. *Power Amplifier*

Wireless transmission through inductive coupling requires a high voltage AC excitation at primary coil. Since batteries produce a much lower voltage, an amplifier is required not only for voltage amplification but also for efficient DC to AC inversion. Class E Power Amplifier (PA) has capability to drive relatively high AC current through the transmitter coil for a relatively low DC input current and voltage with 100% theoretical efficiency.

1) Design Process: The true Class E operation is achieved with 100% theoretical efficiency when the transistor is operated at optimum conditions. Optimum conditions for an amplifier containing a switch and an appropriate load network are described by Raab et al. [9] and Sokal et al. [10], [11]. Analysis of Class E amplifier is straightforward but quite tedious as all the parameters are interrelated. Different analysis methodologies to derive Class E circuit have been reported in literature [9-16]. Comparison of these techniques is given in [17]. Component values for Class E amplifier based on Sokal's explicit design equations are given in Table II. Fig. 5a depicts the complete transmitter design driven by a 5V battery.

TABLE II
CLASS E PARAMETERS

Operating Frequency	*2.5MHz*
Output Power	100mW
Supply Voltage	5V
Inductance – Transmitter Coil	80µH
Parallel Capacitor (C_{shunt})	81pF
Series Resonant Capacitance (C_{series})	66pF
RF choke (L_{choke})	400µH
R_{load}	127Ω



(a)

(b)

Fig. 5. (a) Transmitter Design; (b) Receiver Design

IV. RECEIVER STIMULATOR

Data and power recovery are most essential aspects of the receiver circuitry. Fig. 5b depicts the receiver end of the transcutaneous link with ASK demodulator, power rectifier and low pass filter. In order to decode data, a low-power PIC was used. Digital output from PIC was converted to analogue current signal using a low power D-to-A converter. Using an indigenously developed H-bridge like topology, signal was converted into biphasic pulses. Finally, by using a low-power analogue demultiplexer, electrical pulses were demultiplexed into eight different channels and pulses were provided to electrode array in interleaved fashion. Fig. 6 depicts receiver-stimulator block diagram.

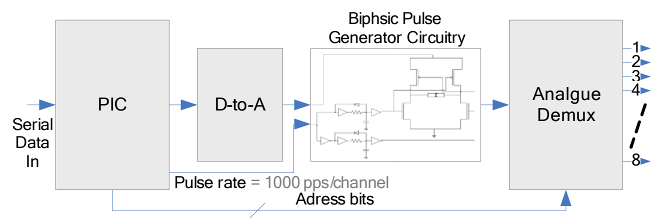


Fig. 6. Logic and stimulator block diagram

V. SIMULATION AND RESULTS

Fig. 7 depicts link simulation of the optimum inductive link topology in SPICE. The inductive link behaves as a band pass filter at the central frequency of 2.5MHz.

Fig. 8a shows switching signal given by DSP, while Fig. 8b and 8c show waveforms of the ASK modulated signal at the gate of PA.

Class E waveforms are shown in Fig. 9. Upper waveform is that of the gate signal with 50% duty cycle and 2.5MHz switching frequency, whereas the lower graph shows the drain to source voltage, V_{DS} of the transistor. Waveforms show true Class E operation with zero voltage at drain when the switch is closed. Voltage, current product at any time in complete cycle is nearly zero which results in approximately 100% amplifier efficiency. Fig. 9c and 9d show voltage across the primary coil which is nearly 40V_{pp} at high state.

Fig. 10 depicts the voltage waveforms at the secondary side. 6V regulated DC output voltage was acquired at the secondary side. Data rate up to 128kbps was achieved with 36mW output power, which implies 36% link efficiency.

Fig. 11 shows final output in the form of biphasic electrical pulses of the first four successive channels.

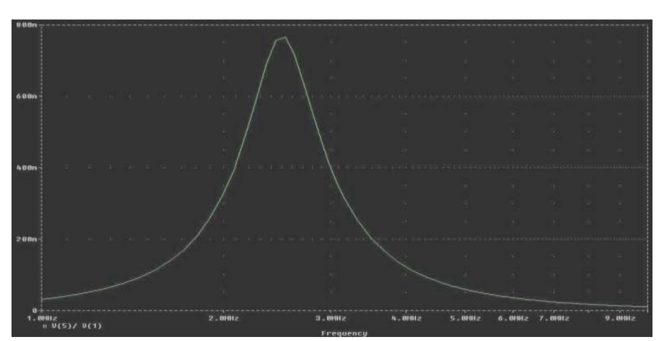


Fig. 7. Link Simulation in SPICE. Horizontal scale depict frequencies and vertical scale depicts voltage gain

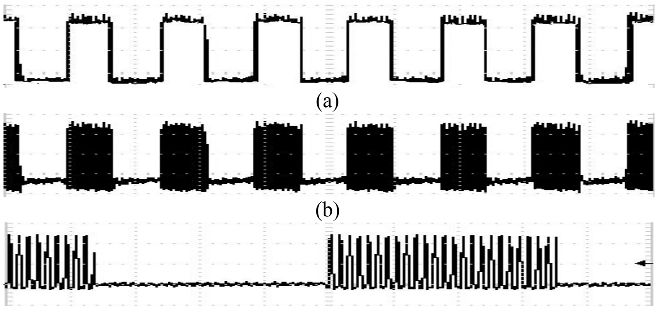


Fig. 8. Voltage Waveforms of the modulating transistor (a) Gate Signal, (b) ASK modulated signal at drain, (c) close view of the ASK modulated signal

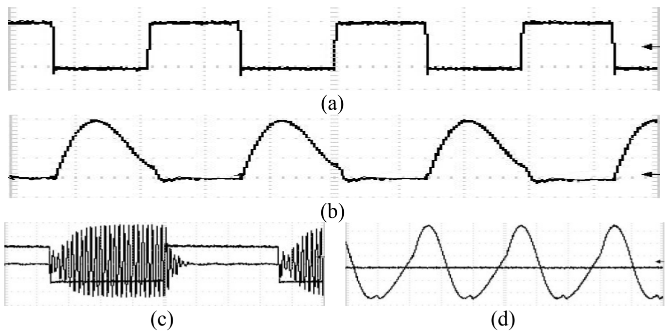


Fig. 9. Class E Waveforms. (a) V_{gate} (b) drain to source voltage V_{DS} (c)Data signal at the gate (x6) and voltage across primary coil (d)Voltage across primary coil in high state= 40 V_{PP}, time scale = 1.4us

VI. CONCLUSION

Design overview of a low cost prototype of cochlear implant system, developed from commercial off-the-shelf components, has been presented. Prototype is suitable for conducting research and experiments in laboratory environment with different speech processing strategies, transcutaneous link and receiver-stimulator circuitry. Design presented in this paper can be used to develop wireless link at a different carrier frequency which can be optimized for link efficiency, voltage gain, output power and higher data rates by following the given techniques.

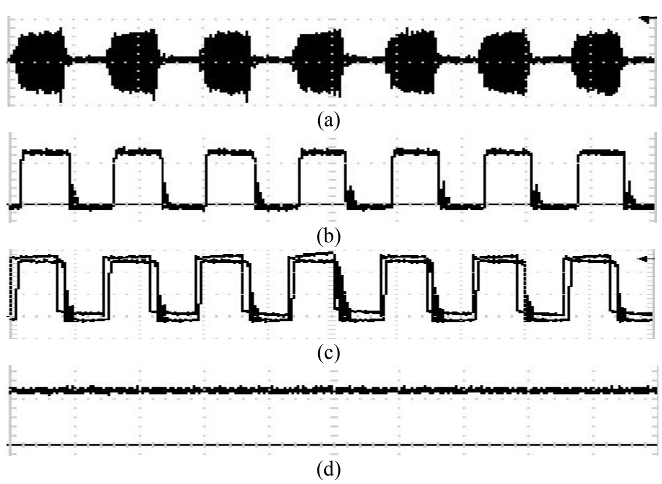


Fig. 10. Waveforms at the secondary side. (a) Voltage at receiver coil, across tuning capacitor, (b)Data output at the demodulator, (c) Comparison of data-IN (DSP output at the primary side) and data-OUT (secondary side), (d) Rectified, regulated output voltage at the secondary side = 6V dc.

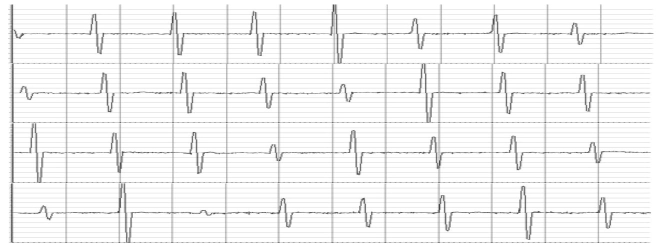


Fig. 11. Interleaved biphasic electrical pulses of the first four channels

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